Confirmation No. 7385

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	BINK *et al.*	Examiner:	Petranek, J.
Serial No.:	10/598,583	Group Art Unit:	2183
Filed:	September 5, 2006	Docket No.:	NL040236US1 (NXPS.583PA)
Title:	ELECTRONIC CIRCUIT FOR REDUCING PIPELINE STAGES DEPENDENT UPON INSTRUCTIONS BEING EXECUTED		

REPLY BRIEF

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Dear Sir:

This is a Reply Brief submitted pursuant to 37 C.F.R. § 41.41(a)(1) for the above-referenced patent application. This Reply Brief is submitted in response to the Examiner's Answer dated May 14, 2010, and in further response to the Final Office Action dated September 29, 2009.

Only if required, authorization is given to charge/credit Deposit Account 50-4019 (NL040236US1) any requisite fees/overages to enter this paper.

I. Status of Claims

Claims 1-20 stand rejected and are presented for appeal.

II. Grounds of Rejection

The grounds of rejection to be reviewed on appeal are as follows:

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) over Hennessy ("Computer Organization and Design: The Hardware/Software Interface") in view of Colwell (U.S. Patent No. 5,604,878).

III. Appellant's Reply Argument

A. The Alleged Correspondence To Claim Limitations Acknowledged As Missing Improperly Relies Upon An "Obvious To Try" Argument.

Appellant's traversals of record established that the cited combination of the Hennessy and Colwell '878 references does not teach claim limitations directed to a latch that is held open for propagating pipeline data in both normal and reduced operation modes, as the cited "pipe extend buffer 60" is not held open in a reduced mode as with the claimed latch. These traversals are further consistent with the Examiner's own indications in confirming that Appellant's "'reduced mode' limitation isn't explicitly taught by" the '878 reference (see page 13 of the Examiner's Answer). Accordingly, the cited combination of references fails to teach limitations including those in claim 1 (by way of example) directed to an electronic circuit that operates in both a normal mode in which a latch is opened/closed in response to an enable signal, and a reduced mode in which the enable signal is overridden by a control signal to hold the latch open for pipeline data to propagate through the latch, independently from the enable signal.

The Examiner's Answer attempts to rebut this lack of correspondence by explaining how some undisclosed system involving the cited combination of references might function in view of Appellant's claims. The Examiner attempts to support this undisclosed system by asserting that the "recent KSR ruling" somehow permits the Examiner to concoct an embodiment that is nonexistent in the prior art. Referring to page 14 of the Examiner's Answer, the Examiner alleges a complicated scenario in which one of ordinary skill would:

1) "realize that there are a finite number of ways for an ALU type instruction to bypass the MEM/WB pipeline register to allow for early retirement in the fifth clock cycle" and that

2) "[o]ne of these ways would be to allow the MEM/WB pipeline register to be kept open during the fifth clock cycle as detailed above (i.e., the fourth executed clock cycle of the subtraction instruction), which allows for the ALU result to flow out of the MEM/WB pipeline register, through the MUX, and be written into the register file during the fifth clock cycle as detailed above (i.e., the fourth executed clock cycle of the subtraction instruction.")

In reply, Appellant submits that this attempt to show correspondence fails to either establish that the alleged "finite" number of ways in item "1" above were known, or that the prior art either disclosed or suggested the complicated scenario in item "2." This attempt to allege correspondence stands in stark contrast to the requirements of Section 103(a) and the tenets of the *KSR* decision, which were clarified by the *Kubin* court (citing *KSR*) in confirming that the cited references should contain detailed enabling methodology for practicing the claimed invention, a suggestion to modify the prior art to practice the claimed invention, and evidence suggesting that it would be successful. [1,2] As applicable here, the Examiner's assertion that obviousness can be established by showing that a person of ordinary skill would "pursue the known options" fails because the Examiner has not established that the asserted options missing in the cited references were "known" (in item "1" above) or that one of skill in the art would modify the references in accordance with the complicated scenario in item "2" above. The Examiner's assertions further fail as the proposed combination would involve the use of a multiplexer 61 in the '878 reference to either select or bypass the pipe extend buffer 60 (*see* Figure 3 and column 7:60-63). The record is silent as to any evidence supporting the Examiner's assertion that there are "a finite number of ways for an ALU type instruction to bypass the MEM/WB pipeline register" or for holding a MEM/WB pipeline register open to operate during a specific fifth clock cycle. As such, these examples are not drawn from any "known" option but instead from the Examiner's opinion as to what would be "obvious to try." Such an assertion is contrary to *KSR* and relevant case law. Appellant therefore submits that the rejections fail to establish that claim limitations directed to a reduced mode of operation in which data is propagated through a latch were a "known" option, and thus fail to establish correspondence to the claimed invention as a whole.

[1] *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007)
[2] *In re Kubin*, 561 F.3d 1351 (Fed. Cir. 2009)

B. The Proposed Combination Of References Would Result In An Extended Mode Of Operation That Fails To Correspond To The Claimed Reduced Mode.

As consistent with Appellant's traversals of record, the proposed combination of the Colwell '878 and Hennessy references involves adding a pipe extend buffer 60 after the end of the third pipe stage 43 as shown in Figure 3 of the '878 reference, which uses the buffer 60 to extend the length of the pipeline when writeback conflict exists (*see, e.g.,* Col. 7:55-66). As such, the '878 reference teaches a normal mode and an extended mode, the latter of which involves the pipe extend buffer. These modes of operation fail to correspond to limitations directed to an electronic circuit that has a reduced mode of operation including a truncated passage that bypasses a processing stage of a pipeline (*e.g.,* a latch is held open for the generated pipeline data to propagate through the latch).

The Examiner's Answer expressly acknowledges that the cited combination of references fails to teach the claimed "reduced mode" of operation, and goes on to assert that one of skill in the art would operate the secondary '878 reference by ignoring the primary Hennessy reference with "the output of the pipe extended buffer being selected as operating in the normal mode and the output of element 43 bypassing the pipe extend buffer being selected as operating in the reduced mode." In other words, the Examiner appears to be asserting that the cited "normal" mode in which element 43 bypasses the pipe extend buffer is the claimed reduced mode.

In reply, Appellant submits that this assertion involving the bypass of the pipe extend buffer in the reduced mode is not only unsupported by any evidence, it renders the proposed combination inapplicable because the Examiner relies upon this very extend buffer in asserting correspondence to the claimed reduced mode in the first place. Clearly, the short and long modes as cited involve using the multiplexer 61 to either draw a signal from before or after the pipeline extend buffer 60 (*see* Figure 3 and column 7:55-63). In bypassing the cited buffer with element 43 in the alleged "reduced" mode, data is not propagated through the pipe and there is no correspondence. Accordingly, the § 103(a) rejection of claims 1-20 is improper and Appellant requests that it be reversed.

C. **The Rejections Of Claims 2 And 3 Fail To Establish That The Missing Limitations Are Inherent (Necessarily Present), Thus Failing To Disclose A Latch Control Circuit Configured To Provide An Enable Signal.**

Appellant's traversals established that the cited references do not teach a latch control circuit configured to provide an enable signal to a latch in a normal mode, and to prevent the enable signal from being provided to the latch in a reduced mode. Specifically, the '878 reference does not control the passage of signals through the cited buffer 60 with an enable signal, but rather uses a multiplexer 61 to draw an input from either before or after the buffer. Control logic 62 provides a control signal to the multiplexer 61 to effect the selection of the input. This is consistent with Figure 3 and column 7:55-63 of the '878 reference.

The Examiner's Answer relies upon an unsupported allegation of inherency in asserting that a clock signal is inherently the claimed enable signal, and that the proposed combination also inherently "includes logic to override the clock signal from normally being applied."

In reply, Appellant submits that these assertions of inherency are unsupported by any reference and further not only fail to establish that the missing limitations are necessarily present, they result in an embodiment that does not correspond. First regarding the alleged inherency, the Examiner has failed to show extrinsic evidence that makes "clear that the missing descriptive matter *is necessarily present in the thing described in the reference*, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991) (emphasis added). Specifically, the Examiner has failed to establish that the clock signal (the asserted "enable" signal) would not be provided to the pipe extension buffer 60 in any mode, or that the clock signal would be overridden from being applied. Moreover, these assertions fail because the cited combination actually operates in a different manner, instead using the multiplexer 61 to select a signal from before or after the buffer 60 and thus has no bearing upon any control signal applied to the buffer itself (whether or not the buffer 60 operates, the multiplexer can select the appropriate signal). The '878 reference thus teaches away from the very modification suggested by the Examiner (which is further improper as iterated below in Section D). Accordingly, the § 103(a) rejection of claims 2 and 3 is improper and Appellant requests that it be reversed.

D. The Cited References Teach Away From The Proposed Combination, Which Further Renders The Hennessy Reference Inoperable.

As consistent with Appellant's traversals, the Hennessy reference teaches away from the Examiner's proposed combination, which would undermine the operation of Hennessy, contrary to the recent *KSR* decision and M.P.E.P. § 2143.01. Specifically, the rejection relies upon modifying the Hennessy reference, which is directed to a synchronous pipeline processor in which each stage of the pipeline is controlled by a clock signal, by instead using multiplexer 61 and control logic 62 of the '878 reference (*see* Figure 3) to bypass a MEM/WB stage of Hennessy's pipelined datapath (*see* Figure 6.25). Bypassing the MEM/WB stage would result in the corruption of the data being processed by Hennessy's synchronous pipeline processor because the added multiplexer would effect the output of data from before the MEM/WB stage, prior to the receipt of the next pulse of the clock signal, changing the input data to the subsequent pipeline stage before that stage finishes processing the current data.

The Examiner's Answer attempts to address Appellant's traversals by asserting that "[a]ny ALU instruction following a store instruction in Hennessy is needlessly delayed by a clock cycle from writing to the register file for simplicities sake in ensuring that no writeback contentions occur." The Examiner's Answer further asserts that "the control logic of Colwell [is used] to ensure that no corruption occurs."

In response, Appellant submits that this answer completely ignores Appellant's traversals regarding the provision of data from before the MEM/WB stage to a point after the MEM/WB stage, and that the assertion that the control logic of Colwell is used to ensure that no corruption occurs is completely devoid of any explanation as to how the Colwell '878 reference would be or could be used to do so. Accordingly, the Examiner's Answer failed to explain how the primary Hennessy reference could or would operate as modified, and has failed to refute Appellant's traversals regarding the teaching away in the cited references.

Appellant's traversals further noted that the Examiner mischaracterized the teachings of the '878 reference in asserting that "(w)hen the ALU instruction reaches the fourth pipeline stage, the control logic of Colwell [the '878 reference] determines that no conflict occurs in the fifth pipeline stage and that the ALU instruction can wire its data a clock cycle early to the register file." As consistent with the above discussion in Section A, the '878 reference does not teach that the control logic 62 allows for bypassing pipeline stages in the middle of Hennessey's

synchronous pipeline processor, and instead uses a pipe extend buffer 60 after the end of the third pipe stage 43 to extend the pipeline, with the flow controlled by a multiplexer 61. *See, e.g.,* Figure 3.

The Examiner's Answer attempts to address these traversals by asserting that a "pipe extend buffer that extends a pipeline stage for Fadd instructions is the exact same method of Hennessy extending the pipeline by a stage for ALU type instructions by adding the MEM/WB pipeline register." The Examiner's Answer goes on to assert that "[t]he only difference between the two references is that Hennessy uses the MEM/WB pipeline register to extend every ALU type instruction … and that Colwell uses the bypass logic to selectively extend Fadd type instructions."

In reply, Appellant first submits that, by the Examiner's own assertions, the respective references do not disclose the "exact same method" as there are differences in the references. Moreover, the Examiner's Answer does not address Appellant's traversals indicating that the '878 reference does not teach bypassing pipeline stages in the middle of a synchronous pipeline processor. As discussed above, the '878 reference would involve adding a buffer (60) at the end of a pipeline. Accordingly, as the record stands, the proposed combination does not involve bypassing pipeline stages in the middle of a pipeline processor as asserted.

In view of the above, the Hennessy reference teaches away from the Examiner's proposed modification, which renders the Hennessy reference inoperable. As such, there is no motivation for the skilled artisan to modify Hennessy in such a manner and Appellant requests that the § 103(a) rejections be reversed.

IV. Conclusion

In view of the above and the underlying Appeal Brief, Appellant submits that the rejections of claims 1-20 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

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